SWITCH CONTROL CIRCUIT AND SWITCH CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-051324, filed March 13, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a switch control circuit and a switch circuit.

BACKGROUND

Recently, wireless communication that uses frequencies with a plurality of bandwidths has been performed. At this time, a switch circuit IC which is obtained by integrating a plurality of high-frequency switches into one-package is used. In the switch circuit IC, if, while communication is performed through a signal path of one frequency bandwidth, a signal path of another frequency bandwidth is switched, there is a possibility that a power supply potential that is supplied to a signal path through which communication is performed temporarily varies, and insertion loss and high-frequency characteristics of the high-frequency switch are temporarily degraded.

An example of related art includes JP-T-2005-515657.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating a schematic configuration of a switch circuit according to an embodiment.

FIG. 2 is a circuit diagram illustrating an example of an internal configuration of one switch group.

FIG. 3 is a block diagram illustrating an example of an internal configuration of one cut-off circuit.

FIG. 4 is a signal waveform diagram of each unit in a switch control circuit.

FIG. 5 is a signal waveform diagram according to one modification example of FIG. 4.

FIG. 6 is a signal waveform diagram according to another modification example of FIG. 4.

FIG. 7 is a signal waveform diagram according to still another modification example of FIG. 4.

DETAILED DESCRIPTION

[0004]

Embodiments provide a switch control circuit and a switch circuit which are configured in such a manner that variation of a power supply due to switching of a signal does not occur.

[0005]

In general, according to one embodiment,

[0007]

Hereinafter, embodiments will be described with reference to the drawings. The following embodiments will be described with a focus on characteristic configurations and operations of a switch control circuit and a switch circuit, but configurations and operations which are omitted in the following description may exist in the switch control circuit and the switch circuit. However, such omitted configurations and operations are also included in the scope of the present embodiments.

[0008]

FIG. 1 is a block diagram illustrating a schematic configuration of a switch circuit 1 according to an embodiment. The switch circuit 1 in FIG. 2 includes a plurality of switch groups 2, and a switch control circuit 3 that controls the switch groups 2.

[0009]

The switch control circuit 3 includes a plurality of drivers (first voltage generation circuit) 4, a plurality of cut-off circuits 5, a control circuit 6, an internal voltage generation circuit (second voltage generation circuit) 7, and a decoder 8.

[0010]

The plurality of drivers 4 generates a plurality of second control signals that level-shifts a plurality of first control signals that is output from the decoder 8, using an internal voltage (reference voltage) Vn that is generated by the internal voltage generation circuit 7. The plurality of cut-off circuits 5 switches whether to supply an internal voltage to the plurality of drivers 4 or not.

[0011]

The control circuit 6 changes a signal logic of either of cut-off control signals Vcut1 and Vcut2 which is input to a corresponding cut-off circuit 5 among the plurality of cut-off circuits 5, for a predetermined period, with respect to the driver 4 other than the drivers 4 to which the first control signal whose signal logic is changed is input. That is, when a signal logic of at least one of the plurality of the first control signals is changed, the control circuit 6 controls the cut-off circuit 5, in such a manner that the reference voltage which is supplied to at least one of a plurality of first voltage generation circuits to which the others of the plurality of the first control signals are input is cut off for a predetermined period. While a signal logic of either of the cut-off control signals Vcut1 and Vcut2 which is input is changed, the cut-off circuit 5 stops supplying of the reference voltage to the corresponding driver 4. The predetermined period is, for example, several m seconds to several tens of m seconds.

[0012]

As illustrated in FIG. 1, the internal voltage generation circuit 7 includes a ring oscillator circuit 11, a charge pump circuit 12, and a regulator circuit 13. The ring oscillator circuit 11 generates an oscillation signal with a predetermined frequency. The charge pump circuit 12 generates a voltage that is obtained by increasing or decreasing a power supply voltage, using the power supply voltage and the oscillation signal that is supplied from the switch circuit 1. The regulator circuit 13 generates an internal voltage by performing waveform shaping or the like of the voltage that is generated by the charge pump circuit 12. The internal voltage Vn that is generated by the internal voltage generation circuit 7 illustrated in FIG. 1 is, for example, a negative potential that is lower than a ground potential. The internal voltage is, for example, approximately -3 V.

[0013]

Generating the second control signal for driving the switch group 2 by using a negative potential in the present embodiment is for decreasing a threshold value of each switch that configures the switch group 2 as much as possible, decreasing an ON resistance, and reducing insertion loss of a switch. When the threshold value of a switch is decreased to approximately 0 V, in order to reliably turn off the switch, it is necessary to supply a negative potential. Thus, the present embodiment generates the second control signal by using a negative potential.

[0014]

While omitted in FIG. 1, the internal voltage generation circuit 7 that generates an internal voltage higher than the power supply voltage may be provided separately. Alternatively, an internal voltage higher than the power supply voltage may be input from the outside of the switch circuit 1.

[0015]

The decoder 8 decodes an input control signal that is input from the outside of the switch circuit 1, and generates a plurality of the first control signals. The decoder 8 is not essential, and may directly input the plurality of the first control signals from the outside of the switch circuit 1.

[0016]

Each of the plurality of the switch groups 2 includes a plurality of switches that switch to connect any one of a plurality of ports P11 to P1n and P21 to P2m to common signal ports P10 and P20, based on a plurality of the second control signals. Antennas ANT1 and ANT2 are respectively connected to common signal ports P10 and P20.

[0017]

FIG. 2 is a circuit diagram illustrating an example of an internal configuration of one switch group 2. The switch group 2 of FIG. 2 is a circuit diagram illustrating an internal configuration of a single-pole 4-throw (SP4T) switch that selects one from among four ports. The SP4T switch performs a switching operation of connecting any one of four RF terminals RF1 to RF4 to a common RF terminal RF\_COM, in response to four second control signals Con1 to Con4.

[0018]

The SP4T switch of FIG. 2 includes a through FET21 that is configured by making a multi-stage series connection of a plurality of FETs between the common RF terminal RF\_COM and each of the four RF terminals RF1 to RF4, and a shunt FET22 that is configured by making a multi-stage series connection of a plurality of FETs between each of the RF terminals and a ground node. A threshold voltage Vth of each FET is, for example, 0 V.

[0019]

Making the multi-stage series connection of the plurality of FETs for each of the through FET21 and the shunt FER22 is for suppressing a voltage that is applied to each FET by sharing a voltage amplitude with the plurality of FETs which are connected in series, because, when signals are transmitted, the RF terminals RF1 to RF4 have a voltage amplitude of several tens of volts.

[0020]

For example, an operation of the SP4T switch of FIG. 2 will be described by using a case in which the RF terminal RF1 is connected to the common RF terminal RF\_COM, as an example. In this case, the second control signal Con1 becomes a high potential (Von), the through FET21 having a gate to which the second control signal Con1 is input is turned on, and the shunt FET22 that is connected between the RF terminal RF1 and a ground terminal is turned off. In addition, the others of the through FET21 are all turned off, and the others of the shunt FET22 are all turned on.

[0021]

A potential Von of the second control signal Con1 may be a potential that is obtained when the through FET21 is turned on and thereby an ON resistance thereof becomes small enough. The potential Von is, for example, 3 V. Potentials Voff of the second control signals Con2 to Con4 are a gate potential which can be maintained in a cut-off state of the through FET21, even if the RF signal is input to the RF terminals RF2 to RF4. The potential Voff is the voltage Vn that is generated by the internal voltage generation circuit 7 of FIG. 1, and is, for example, -3 V.

[0022]

Even if the through FET21 is turned off, a leakage current is generated through an OFF capacitor in a high-frequency switch circuit 12 of FIG. 2, but the leakage current flows through the shunt FET22.

[0023]

Two switch groups 2 are illustrated in FIG. 1, but particularly the number of the switch groups is not limited. For example, if, while wireless communication is performed by using a port that is selected by the witch group 2 on an upper side of FIG. 1, a port is switched by the switch group 2 on a lower side, there is a possibility that the internal voltage Vn output from the internal voltage generation circuit 7 which is supplied to the driver 4 that is connected to the switch group 2 on the upper side varies at the moment when the port is switched. The driver 4 generates the second control signal that is obtained by level-shifting the first control signal, using the power supply voltage on a negative side which is supplied from the internal voltage generation circuit 7, and the power supply voltage on a positive side which is supplied from an internal voltage generation circuit or the like that is not illustrated. However, at the moment when the port is switched, a voltage on a negative side of the second control signal of the switch group 2 increases, and the power supply voltage on a negative side varies due to the influence. If the power supply voltage on a negative side varies, a voltage level on a negative side of the second control signal of another switch group 2 is increased, harmonic characteristics and insertion loss of such another switch group 2 are instantaneously degraded. In this way, there is a possibility that, at the moment when a port is switched, the voltage level on a negative side of the second control signal that is output from the driver 4 is increased.

[0024]

Thus, in the present embodiment, the cut-off circuit 5 is connected between each driver 4 and the internal voltage generation circuit 7, a port is switched by the cut-off circuit 5 in the driver 4 that is connected to the switch group 2 which does not perform switching of a port, and thereby an internal voltage is not supplied for a predetermined period.

[0025]

All the switch groups 1 of FIG. 1 may be embedded in one IC. Alternatively, all the switch control circuits 3 may be embedded in one IC, and the switch groups 2 may be embedded in another IC. If integrated into an IC, it is preferable that the switch circuit 1 is formed on a silicon on insulator (SOI) substrate rather than a silicon substrate. The reason is that the SOI has a MOS transistor with a parasitic capacitor smaller than that of the silicon substrate, and in addition has small power loss of a high-frequency signal.

[0026]

FIG. 3 is a block diagram illustrating an example of an internal configuration of one cut-off circuit 5. The cut-off circuit 5 of FIG. 3 includes a level shifter 31 and a switching element 32. The level shifter 31 outputs either a potential higher than both of the internal potential Vn that is output from the internal voltage generation circuit 7 in accordance with a potential of the cut-off control signal Vcut that is output from the control circuit 6, and the internal potential Vn that is supplied from an internal circuit which is not illustrated, or the ground potential, and supplies the potential to the gate of the switching element 32.

[0027]

The switching element 32 is, for example, an NMOS transistor. Thus, if the gate increases to a voltage equal to or higher than a threshold voltage, compared to a source thereof to which a gate voltage is applied, the switching element 32 is turned on.

[0028]

For example, if the control signal Vcut is in a high level and the internal voltage Vn is -3 V, a voltage level of the control signal Vcut is level-shifted up to a voltage level (for example, approximately 0 V) higher than the threshold voltage of the switching element 32, so as to reliably turn off the switching element 32. By doing this, if the control signal Vcut is in a high level, the switching element 32 is turned off, and the internal voltage Vn is not supplied to the driver 4.

[0029]

FIG. 4 is a signal waveform diagram of each unit in the switch control circuit 3. FIG. 4 illustrates an example in which switching of a port is performed by the switch group 2 on an upper side of FIG. 1, at the time of time TSW. The control circuit 6 senses whether or not the switching of a port is performed. The control circuit 6 monitors the input control signals Vc1 and Vc2 to the decoder 8, and identifies which driver 4 the logic change corresponds to, if logics of the input control signals Vc1 and Vc2 are changed. Then, signal logics of the control signals Vcut1 and Vcut2 that command cut-off of the internal voltage Vn are switched with respect to the cut-off circuit 5 which is connected to the driver 4. In FIG. 4, if port switching of the switch group 2 on an upper side is sensed at the time TSW, the control circuit 6 changes the control signal Vcut2 from low to high. By doing this, the cut-off circuit 5 that is connected to the driver 4 on a lower side stops supplying of an internal voltage to the driver 4 on the lower side for a predetermined period (up to time Tsw1). The predetermined period is a short period of several m seconds to several tens of m seconds, and even if the internal voltage Vn output from the internal voltage generation circuit 7 is not supplied to a power supply voltage lines of the driver 4 within the period, there is no possibility that the power supply voltage lines are rapidly changed. In the signal waveform diagram of FIG. 4, the power supply voltage lines of the driver 4 on the lower side become substantially the same potential as each other in approximately the time Tsw1.

[0030]

Meanwhile, the cut-off circuit 5 that is connected to the driver 4 corresponding to the switch group 2, which performs switching of a port, on an upper side of FIG. 1 does not cut off the internal voltage Vn, and thus, the negative potential Vn1 of the switch group 2 is rapidly increased by the port switching of the switch group 2. According to this, the internal voltage Vn that is supplied to the driver 4 on the upper side rapidly increases at the time TSW. However, the rapid voltage change is temporary, and in addition, wireless communication is not performed immediately after the port is switched, and thus practical problems do not occur.

[0031]

It is preferable that a length of the predetermined period in which supplying of an internal voltage is stopped by the cut-off circuit 5 is set to an optimal length by taking into account a voltage level of the internal voltage, a parasitic capacitance of the power supply voltage line of the driver 4, or the like.

[0032]

After the predetermined period is ended, it is not necessary to take action, in such a manner that a temporary increase of the power supply voltage line does not all occur.

[0033]

FIG. 5 is a signal waveform diagram according to a modification example of FIG. 4. In FIG. 5, at the time Tsw1 when the predetermined period in which supplying of the internal voltage is stopped by the cut-off circuit 5 is ended, an example in which the power supply voltage line of the driver 4 on the lower side slightly increases is illustrated. In the example of FIG. 5, while a voltage in a normal state is Vn\_static, the voltage slightly increases up to Vn\_swoff at the time of Tsw1. However, although the power supply voltage line of the driver 4 on the lower side slightly increases, if the second control signal that is generated by the driver 4 on the lower side can correctly turn on or off the switch group 2 on a subsequent stage side thereof, there is no practical problem.

[0034]

In this way, the length of the predetermined period may be set within a range in which unintended activation of a switching operation of the switch group 2 is not performed.

[0035]

The control circuit 6 of FIG. 1 controls cut-off timing of a plurality of cut-off circuits 5, based on the input control signal that is input to the decoder 8, but as illustrated in FIG. 6, may control cut-off timing of the plurality of cut-off circuits 5, based on a plurality of first control signals that is output from the decoder 8. When an arbitrary switch group 2 from among a plurality of switch groups 2 performs switching of a port, a signal logic of any one of the plurality of the first control signals is changed. Thus, when monitoring the plurality of the first control signals, the control circuit 6 can detect simply and easily the cut-off circuit 5 that has to be cut off from among the cut-off circuits 5 connected to the driver 4.

[0036]

However, there is a possibility that the number of the plurality of the first control signals which is output from the decoder 8 is considerably more than the number of the input control signals that are input to the decoder 8. Thus, when the control circuit 6 monitors the plurality of the first control signals, the number of the input signals of the control circuit 6 is increased more than that in FIG. 1.

[0037]

Meanwhile, in FIG. 1, the control circuit 6 has to perform decoding processing of the input control signal, and an internal configuration of the control circuit 6 becomes complicated. Thus, a configuration of either FIG. 1 or FIG. 6 may be selected by the number of bits of the input control signals, the number of the plurality of the first control signals, or the like.

[0038]

In addition, a control circuit 6 of FIG. 7 is also considered as an intermediate configuration between FIG. 1 and FIG. 6. The decoder 8 of FIG. 7 generates the plurality of the first control signals by decoding the input control signal, and generates a third control signal for the control circuit 6. The control circuit 6 of FIG. 7 controls cut-off timing of the plurality of the cut-off circuits 5, based on the third control signal. For example, the number of the third control signals is greater than that of the input control signals, and is smaller than that of the plurality of the first control signals. Thus, in some cases, the internal configuration of the control circuit 6 can be simplified more than that of FIG. 1 or FIG. 7.

[0039]

In this way, in the present embodiment, when switching of a port is performed by any one of the plurality of switch groups 2 that can simultaneously perform wireless communication, the internal voltage Vn is not supplied for a predetermined period to the driver 4 that is connected to the switch group 2 which does not perform the switching of a port. Thus, there is no abnormality in which the internal voltage Vn that is supplied to the switch group 2 which does not perform the switching of a port varies greatly under the influence of the switching of a port. Thus, it is possible to reduce off distortion of the switch groups 2 that are connected to the other drivers 4, and unintended activation of switching of the switch group 2 is not generated. Thus, when the switching of a port is performed by a certain switch group 2, insertion loss of the other switch groups 2 is not increased, and degradation of high-frequency characteristics can be suppressed.

[0040]

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A switch control circuit comprising:

a first voltage generation circuit that generates a plurality of second control signals which is obtained by level-shifting a plurality of first control signals, using a reference voltage;

a plurality of cut-off circuits that switches whether to supply the reference voltage to the plurality of the first voltage generation circuits or not; and

a control circuit that, when a signal logic of at least one of the plurality of the first control signals is changed, controls the cut-off circuits, in such a manner that the reference voltage which is supplied to at least one of the plurality of the first voltage generation circuits to which the others of the plurality of the first control signals are input is cut off for a predetermined period.

2. The circuit according to Claim 1, further comprising:

a second voltage generation circuit that generates the reference voltage,

wherein the control circuit generates a plurality of cut-off control signals that controls switching of the plurality of cut-off circuits, and

wherein the plurality of cut-off circuits switches whether to supply the reference voltage that is generated by the second voltage generation circuit to a corresponding first voltage generation circuit or not, based on the plurality of cut-off control signals.

3. The circuit according to Claim 1 or 2, wherein the reference voltage is a negative potential that is lower than a ground potential.

4. The circuit according to any one of Claims 1 to 3, further comprising:

a decoder that decodes an input control signal and generates the plurality of the first control signals,

wherein the control circuit generates the plurality of cut-off control signals that controls switching of the plurality of cut-off circuits, based on the input control signal.

5. The circuit according to any one of Claims 1 to 3, further comprising:

a decoder that decodes an input control signal and generates the plurality of the first control signals,

wherein the control circuit generates the plurality of cut-off control signals that controls switching of the plurality of cut-off circuits, based on the plurality of the first control signals.

6. The circuit according to any one of Claims 1 to 3, further comprising:

a decoder that decodes an input control signal and generates the plurality of the first control signals and a third control signal that is supplied to the control circuit,

wherein the control circuit generates the plurality of cut-off control signals that controls switching of the plurality of cut-off circuits, based on the third control signal.

7. A switch circuit comprising:

a plurality of switch groups; and

a switch control circuit that controls the plurality of switch groups,

wherein the switch control circuit includes

a plurality of first voltage generation circuits that generates a plurality of second control signals which is obtained by level-shifting a plurality of first control signals, using a reference voltage;

a plurality of cut-off circuits that switches whether to supply the reference voltage to the plurality of the first voltage generation circuits or not; and

a control circuit that, when a signal logic of at least one of the plurality of the first control signals is changed, controls the cut-off circuits, in such a manner that the reference voltage which is supplied to at least one of the plurality of the first voltage generation circuits to which the others of the plurality of the first control signals are input is cut off for a predetermined period, and

wherein each of the plurality of switch groups includes a plurality of switches that is connected to a common signal port by switching one of a plurality of ports, based on the plurality of the second control signals.

ABSTRACT

According to one embodiments, a switch control circuit includes a first voltage generation circuit that generates a plurality of second control signals which is obtained by level-shifting a plurality of first control signals, using a reference voltage; a plurality of cut-off circuits that switches whether to supply the reference voltage to the plurality of the first voltage generation circuits or not; and a control circuit that, when a signal logic of at least one of the plurality of the first control signals is changed, controls the cut-off circuits, in such a manner that the reference voltage which is supplied to at least one of the plurality of the first voltage generation circuits to which the others of the plurality of the first control signals are input is cut off for a predetermined period.

Drawings

FIG. 1

11: RING OSCILLATOR CIRCUIT

12: CHARGE PUMP CIRCUIT

7: INTERNAL VOLTAGE GENERATION CIRCUIT

13: REGULATOR CIRCUIT

6: CONTROL CIRCUIT

5: CUT-OFF CIRCUIT

k bit INPUT

8: DECODER

4: DRIVER

2: SWITCH GROUP

5: CUT-OFF CIRCUIT

4: DRIVER

2: SWITCH GROUP

FIG. 3

7: INTERNAL VOLTAGE GENERATION CIRCUIT

31: LEVEL SHIFTER

4: DRIVER

FIG. 4

SEVERAL msec TO SEVERAL TENS OF msec

TIME

FIG. 5

SEVERAL msec TO SEVERAL TENS OF msec

TIME

FIG. 6

11: RING OSCILLATOR CIRCUIT

12: CHARGE PUMP CIRCUIT

7: INTERNAL VOLTAGE GENERATION CIRCUIT

13: REGULATOR CIRCUIT

6: CONTROL CIRCUIT

5: CUT-OFF CIRCUIT

k bit INPUT

8: DECODER

4: DRIVER

2: SWITCH GROUP

5: CUT-OFF CIRCUIT

4: DRIVER

2: SWITCH GROUP

FIG. 7

11: RING OSCILLATOR CIRCUIT

12: CHARGE PUMP CIRCUIT

13: REGULATOR CIRCUIT

7: INTERNAL VOLTAGE GENERATION CIRCUIT

6: CONTROL CIRCUIT

5: CUT-OFF CIRCUIT

k bit INPUT

8: DECODER

4: DRIVER

2: SWITCH GROUP

5: CUT-OFF CIRCUIT

4: DRIVER

2: SWITCH GROUP